

CLAIMS

What is claimed is:

- 1 1. A method for testing cache performance of a processor design, the method
2 comprising:
3 searching a file that contains test results for a lot of wafers; and
4 identifying at least one processor on one of the wafers in the lot in which a
5 cache array has passed a cache test.
- 1 2. The method of claim 1, wherein the identifying the at least one processor
2 comprises identifying that a built-in-self-test (BIST) engine in the at least one
3 processor was able to execute the cache test.
- 1 3. The method of claim 1, further comprising identifying all of the processors in
2 the lot in which a cache array has passed the cache test.
- 1 4. The method of claim 3, wherein the identifying all of the processors comprises
2 identifying that a built-in-self-test (BIST) engine in each of the processors was able to
3 execute the cache test.
- 1 5. The method of claim 1, wherein the searching the file comprises parsing the
2 file.
- 1 6. The method of claim 1, wherein the searching the file comprises opening the
2 file and parsing the file.

- 1 7. The method of claim 1, wherein the searching the file comprises
- 2 decompressing the file.

1 8. A system for testing cache performance of a processor design, the system
2 comprising:
3 a parser module for searching a file that contains test results for a lot of wafers;
4 and
5 a cache-testable processor identification module for identifying processors on
6 wafers in the lot in which a cache array has passed a cache test.

1 9. The system of claim 8, wherein the parser module is configured to open the
2 file that contains the test results.

1 10. The system of claim 8, wherein the parser module and the cache-testable
2 processor identification module comprise software that is executed by a processor.

1 11. The system of claim 8, wherein the cache-testable processor identification
2 module is configured to identify the processors for which a built-in-self-test (BIST)
3 engine was able to execute the cache test.

1 12. The system of claim 8, wherein the parser module and the cache-testable
2 processor identification module comprise a PERL script.

1 13. A computer program embodied in a computer-readable medium, the program
2 comprising:

3 logic configured to search a file that contains test results for a lot of wafers;

4 and

5 logic configured to identify at least one processor on one of the wafers in the
6 lot in which a cache array has passed a cache test.

1 14. The computer program of claim 13, wherein the logic configured to identify
2 the at least one processor comprises logic configured to identify that a built-in-self-
3 test (BIST) engine in the at least one processor was able to execute the cache test.

1 15. The computer program of claim 13, wherein the logic configured to search the
2 file comprises logic configured to parse the file.

1 16. The computer program of claim 13, wherein the logic configured to search the
2 file comprises logic configured to decompress the file.

- 1 17. A system for testing cache performance of a processor design, the system
- 2 comprising:
- 3 means for searching a file that contains test results for a lot of wafers; and
- 4 means for identifying all processors on wafers in the lot in which a cache array
- 5 has passed a cache test.